AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A CMOS image sensor, comprising:

an image capturing means for converting rays of light incident upon photosensitive area from an object to an analog signal;

an analog-to-digital converter for converting the analog image signal to a digital value; and

a ramp signal generator for providing ~~producing~~ a ramp signal ~~in order to provide a reference voltage signal~~ to the analog-to-digital converter as a reference voltage signal, the ramp signal generator including:

a plurality of capacitors and switches;

an amplifier coupled to the plurality of capacitors and switches, for receiving gain and reset voltages from an external circuit; and

capacitance controlling means coupled in parallel to at least one capacitor in the ramp signal generator in order to ~~form~~ adjust the ramp signal for ~~an analog~~ a gamma correction.

2. (Original) The CMOS image sensor as recited in claim 1, wherein the plurality of switches in the ramp signal generator are selectively connected in response to control signals from a digital controller in the CMOS image sensor.

3. (Original) The CMOS image sensor as recited in claim 2, wherein the capacitance controlling means includes a plurality of capacitors and a plurality of switches selectively connecting the capacitors in response to the control signal from the digital controller.

4. (Original) The CMOS image sensor as recited in claim 2, further comprising:

counting means for creating a digital value based on a result signal from the chopper comparator; and

a latch circuit for storing the digital value from the counting means.

5. (Amended) A CMOS image sensor, comprising:

an image capturing means for capturing an image for analog image signal from an object;

an analog-to-digital converter to convert the analog image signal to a digital value; and

a ramp signal generator providing ~~producing~~ a ramp signal ~~in order to provide a reference voltage signal~~ to the analog-to-digital converter as a reference voltage signal, said ramp signal generator including:

a first switch connected to a gain voltage;

a plurality of second switches connected in parallel to the first switch;

a plurality of capacitors connected to the second switches;

a third switch connected between the first switch and a ground voltage level;

a fourth switch commonly connected to the plurality of capacitors and connected to a reset voltage;

a fifth switch connected to the plurality of capacitors;

an amplifying means for receiving the reset voltage and receiving the gain voltage via the fifth switch for outputting a ramp signal;

a sixth switch connected in parallel to the amplifying means; and

a capacitor connected in parallel to the sixth switch.

6. (Original) The CMOS sensor as recited in claim 5, wherein the plurality of capacitors and switches in the ramp signal generator are selectively connected each other in response to control signals from a digital controller in the CMOS image sensor.

7. (New) A CMOS image sensor, comprising:

a converter for receiving an inputted analog data and a ramp signal to thereby converting the inputted analog data into a digital data throughout a correlated double sampling and a gamma correction; and

a ramp signal generator for providing the ramp signal which is adjusted for the gamma correction.

8. (New) The CMOS image sensor as recited in claim 7, wherein the converter means includes:

a CDS performing unit for performing the correlated double sampling to the inputted analog data; and

a comparison unit for receiving output of the CDS performing unit and the ramp signal to thereby perform the gamma correction.

9. (New) The CMOS image sensor as recited in claim 8, wherein the gamma correction is performed in a digital signal basis.

10. (New) The CMOS image sensor as recited in claim 7, wherein the converter means includes:

a first switch for transmitting the inputted analog data to a first node;

a second switch for transmitting the ramp signal to the first node;

a first capacitor coupled to the second switch and the first node;

a first device for converting a value of the first node;

a second device for converting output of the first means; and

plural capacitors coupled to the first and second devices, each for storing an offset voltage.

11. (New) The CMOS image sensor as recited in claim 10, wherein each of the first and second devices includes an inverter and a switch.

12. (New) The CMOS image sensor as recited in claim 11, wherein the gamma correction is performed in an analog signal basis.

13. (New) The CMOS image sensor as recited in claim 7, wherein the ramp signal generator includes:

a plurality of capacitors and switches;

an amplifier coupled to the plurality of capacitors and switches, for receiving gain and reset voltages from an external circuit; and

a capacitance controller coupled in parallel to at least one capacitor in the ramp signal generator in order to adjust the ramp signal for the gamma correction.

14. (New) The CMOS image sensor as recited in claim 7, wherein the ramp signal generator includes:

a first switch connected to a gain voltage;

a plurality of second switches connected in parallel to the first switch;

a plurality of capacitors connected to the second switches;

a third switch connected between the first switch and a ground voltage level;

a fourth switch commonly connected to the plurality of capacitors and connected to a reset voltage;

a fifth switch connected to the plurality of capacitors;

an amplifier for receiving the reset voltage and receiving the gain voltage via the fifth switch for outputting a ramp signal;

a sixth switch connected in parallel to the amplifier; and

a capacitor connected in parallel to the sixth switch.

15. (New) The CMOS image sensor as recited in claim 7, further comprising an output device for latching output of the converter.

16. (New) The CMOS image sensor as recited in claim 15, wherein the output device includes:

an up-counter for counting a clock pulse;

a multiplexer for selectively transmitting a result of the up-counter in response to output of the converter; and

a latch for latching output of the multiplexer to feed a latched value to the multiplexer.